Roll No.

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E. (Full Time) - END SEMESTER EXAMINATIONS, APRIL / MAY 2025
ELECTRONICS AND COMMUNICATION ENGINEERING
SEMESTER-IV
EC23C05- ANALOG ELECTRONIC SYSTEM DESIGN
(Regulation 2023)

Time:3 hrs **Max.Marks: 100**

CO1	Ability to design negative feedback amplifiers and analyze stabilization techniques
CO2	Ability to apply and design linear and Non-Linear analog circuits using Op Amp.
CO3	Ability to analyze and realize signal conditioning circuits, power amplifiers and converters.
CO4	Ability to select ICs and design circuits for real time applications
CO5	Ability to analyze RC, LC oscillators and tuned amplifiers

BL – Bloom's Taxonomy Levels
(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

PART- A(10x2=20Marks)
(Answer all Questions)

Q.No	Questions	Marks	CO	BL
1	Compute the voltage gain Vo/Vs, for the circuit shown in Figure-1. Given Vcc = 10 V, hfe = 100, hie = 1.1 kΩ.	2	1	L3
2	Calculate the percent change in the closed-loop gain A_f, Let A = 10^6, A_f =85, and β = 0.01999. Assume that the change in the open-loop gain is dA=10^5 (a 10 percent change).	2	1	L2
3	Consider an op-amp used in a voltage follower (buffer) configuration. The input signal is a high-frequency sine wave with amplitude of 10V peak-to-peak and a frequency of 1 MHz. Calculate the required slew rate.	2	2	L3
4	Compute the input bias current and output volage for an inverting amplifier shown in Figure-2. Let the feedback resistor R_f=1MΩ, bias current I_B^+=500nA, I_B^- =650nA. What is the effect of input bias current? How it can be compensated?	2	2	L3
5	Write the condition for oscillation in a Wien Bridge oscillator in terms of the gain of the amplifier and the attenuation of the feedback network.	2	3,5	L2
6	A ring oscillator (Figure-3) with three inverting MOSFET amplifiers generates the sinusoidal signal at 5kHz. Compute the capacitance and 3dB Bandwidth of individual stage assuming g_m of every MOSFET is 2mA/V.	2	3,5	L4
7	In a 4-bit weighted resistor DAC, the digital input is D = 1011_2. The reference voltage V_{ref} is 5V and scaling factor K = 1. What is the output voltage of the DAC for the given input? If the reference voltage is increased to 10V, what will be the new output voltage?	2	4	L2
8	List any four applications of PLL	2	4	L1
9	A tank circuit is constructed using 100 pF Capacitor and 100 μH inductor. If the coil has a loss resistance of 5Ω, determine the resonant frequency and circuit impedance at resonance.	2	5	L2
10	Consider the design of an IF amplifier for FM radio receiver using six synchronously tuned amplifier stages. The 3 dB bandwidth of each stage is 870kHz. Determine the overall bandwidth of the synchronously tuned amplifier.	2	5	L3

PART- B(5x 13=65 Marks)

Q.No	Questions	Marks	CO	BL
11 (a)	Identify the feedback topology for the circuit diagram shown in Figure-4. Draw the circuit schematic of the open loop amplifier (feedforward) amplifier. Find β, A_i, $A_{if} = I_0/I_s$, $A_{vf} = V_0/V_s$, R_i, R_{if}, R_0 and R_{of}. Let R_{c1}=3kΩ, R_{c2}=500Ω, R_s=1kΩ, R'=1.2kΩ, R_{e2}=50Ω, h_{ie}=1.1kΩ and h_{fe}=50.	13	1	L4
	OR			
11(b)	Determine the transresistance gain, input and output impedances of a single-transistor shunt–shunt feedback circuit. Consider the circuit in Figure-5. The transistor parameters are: h_{FE} = 100, $V_{BE(on)}$ = 0.7 V, and V_A =∞. Let V_{CC}=10V,R_S=10kΩ, R_1=51kΩ, R_2=5.5kΩ, R_F=82kΩ, R_C=10kΩ and R_E=0.5kΩ	13	1	L4
12 (a)	(i) Given that the input voltage range is from 0.1 V to 1 V, and the op-amp is ideal, draw the circuit diagram of a log amplifier using an op-amp and a diode. Derive the expression for the output voltage (V_{out}) of the log amplifier in terms of the input voltage (V_{in}) and the relevant component values. Use the derived formula to calculate the output voltage for input voltages of 0.1 V, 0.5 V, and 1 V. Assume diode saturation current I_S=1 μA. State any assumptions made during the derivation. Briefly explain one practical limitation of the designed log amplifier and suggest a possible modification to mitigate this limitation. (ii) An input voltage $V_{in}(t)$=5sin(1000t) V is applied to an op-amp differentiator circuit. The differentiator uses a capacitor of 0.1μF and a resistor of 10 kΩ. Calculate the output voltage $V_{out}(t)$.	13 [8+5]	2	L4
	OR			
12(b)	(i)Find V_0 for the OP-AMP circuit shown in Figure-6. (ii) Evaluate i_1, I_L, i_0 and v_0 for the amplifier circuit shown in Figure-7. Let R_1=10kΩ, R_f=100kΩ and R_L=25kΩ Also analyze the characteristics of I to V converter.	13 [6+7]	2	L4
13 (a)	The LC oscillator circuits, Colpitt oscillator is designed to produce an oscillation frequency of 1 MHz. Draw their circuit diagram, equivalent circuit and derive the expression for the frequency of oscillation. Analyze the impact on oscillation frequencies if a small parasitic capacitance present in parallel with the inductor(s) of both the oscillators. Will the oscillation frequency increase or decrease in each case? Justify your answer using the derived frequency expressions.	13	3	L2
	OR			
13(b)	(i) Analyze the Class A power amplifier in terms of load line characteristics, power dissipation and power conversion efficiency. (ii) Determine the required biasing in a MOSFET class-AB output stage shown in Figure -8. The parameters are V_{DD} = 10 V and R_L = 20Ω. The transistors are matched, and the parameters are K = 0.20 A/V^2 and |VT| = 1V. The quiescent drain current is to be 20 percent of the load current when v_O =5V.	13 [8+5]	3	L2

14 (a)	(i) A security system requires a pulsed output of 5 seconds duration whenever a momentary switch is pressed. Design a monostable multivibrator circuit using an IC 555 timer to fulfill this requirement. Calculate the required value of the external resistor (R) if a capacitor (C) of 10 µF is used to achieve the desired output pulse duration. Describe the behavior of the output pulse duration of a 555 monostable multivibrator when the trigger input is held low for an extended period that is longer than the programmed pulse width. (ii) Draw a basic block diagram of a 3 op-amp instrumentation amplifier. Assuming ideal op-amps and derive the expression for the output voltage.	13 [7+6]	4	L3
	OR			
14 (b)	(i) Elucidate 3-bit R-2R DAC with the switch position corresponds to the binary word 100 and 001. Draw its equivalent circuit and analyze the output voltage for each case. Let the reference voltage be 5V. Also compare between weighted resistor DAC and R-2R DAC. (ii) Draw the functional diagram of the successive approximation ADC. Examine how the correct digital representation is identified using trail and error approach.	13 [7+6]	4	L3
15 (a)	Draw the circuit diagram of a common-emitter transistor single-tuned amplifier and derive the expression for the voltage gain and bandwidth. Examine how the magnitude of the voltage gain varies as the input signal frequency deviates significantly from the resonant frequency	13	5	L3
	OR			
15 (b)	(i) Design and evaluate the results a FET based single tuned amplifier with g_m=5mA/V, r_0=10kΩ, f_0=1MHz, center frequency gain=-10V/V and 3dB bandwidth=10kHz.Assume c_0 is negligible. Also evaluate the Q factor. Does the calculated Q factor is suitable for communication applications? Justify your answer. (ii) Analyze and compare the Synchronously tuned and stagger tuned amplifiers. Suggest any one real time application of tuned amplifiers	13 [7+6]	5	L3

PART- C(1x 15=15Marks)

(Q.No.16 is compulsory)

Q.No	Questions	Marks	CO	BL
16. (i)	Given the MOSFET parameters $g_{m1}=g_{m2}$=4mA/V, and circuit resistances $R_{D1}=R_{D2}$=10kΩ, R_1=1kΩ, and R_2=9kΩ for the circuit shown in Figure-9. Assuming the circuit is intended to function as a series-shunt feedback amplifier, determine the required bias conditions (DC gate-source voltages V_{GS1} and V_{GS2} and drain currents I_{D1} and I_{D2}) for both MOSFETs to achieve the given g_m values. Assume the threshold voltage Vt = 1V for both transistors. Specify appropriate DC supply voltages (V_{DD}) to ensure operation in the saturation region. Derive expressions for the following parameters of the feedback amplifier: open-loop voltage gain (Av), feedback factor (β=Vf/Vo) and closed-loop voltage gain ($A_{vf}=V_o/V_s$).	7	1	L5

(ii)	(x) Consider a three-pole feedback amplifier with a loop gain $$T(f)=\frac{2000}{(1+j\frac{f}{10^4})(1+j\frac{f}{10^6})(1+j\frac{f}{10^8})}$$ Insert a dominant pole, assuming the original poles do not change, such that the phase margin is at least 45 degrees. Evaluate the dominant pole required to stabilize the feedback system. (y) Determine the required feedback transfer function β to yield a specific phase margin of 45 degrees and determine the resulting closed-loop low-frequency gain. Consider a three-pole feedback amplifier with a loop gain function given by $$T(f)=\frac{\beta(1000)}{(1+j\frac{f}{10^3})(1+j\frac{f}{5X10^4})(1+j\frac{f}{10^6})}$$	8 [4+4]	1	L5

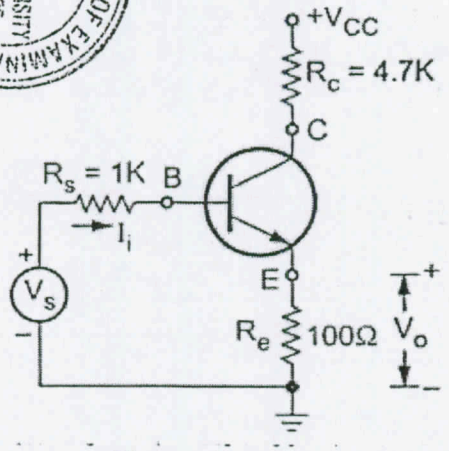

Figure-1

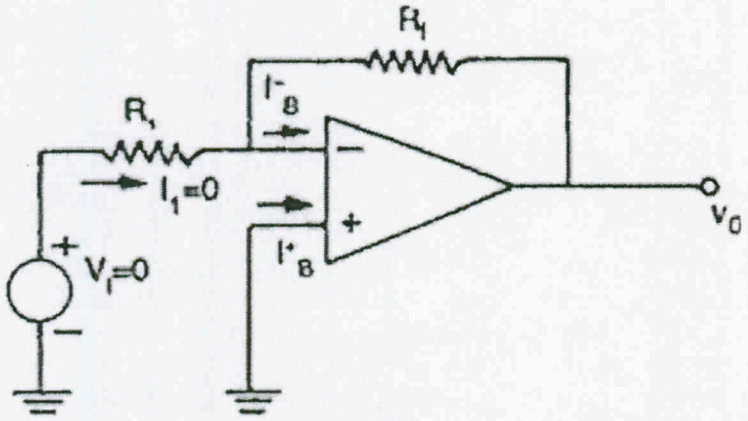

Figure-2

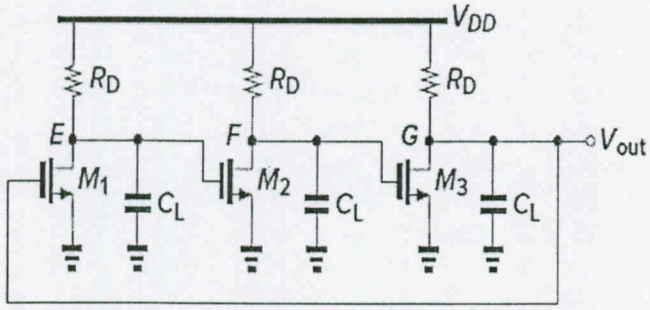

Figure-3

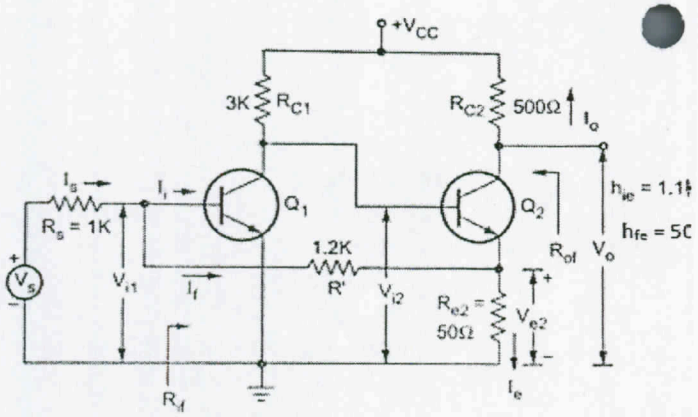

Figure-4

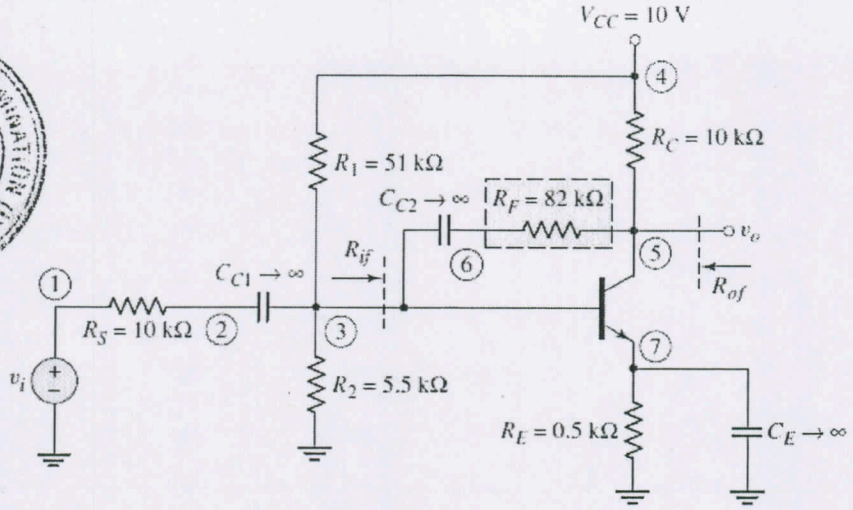

Figure-5

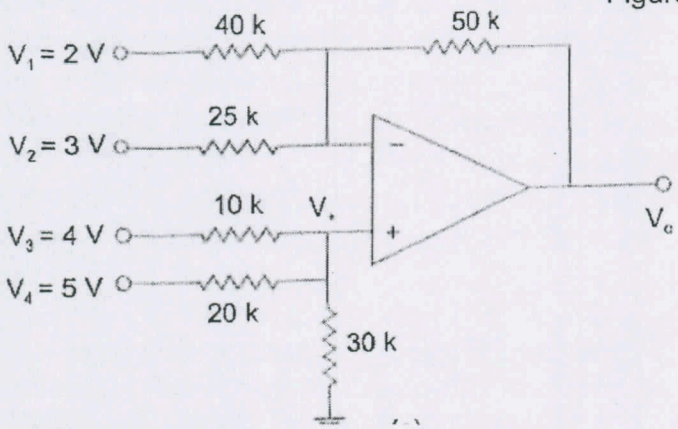

Figure-6

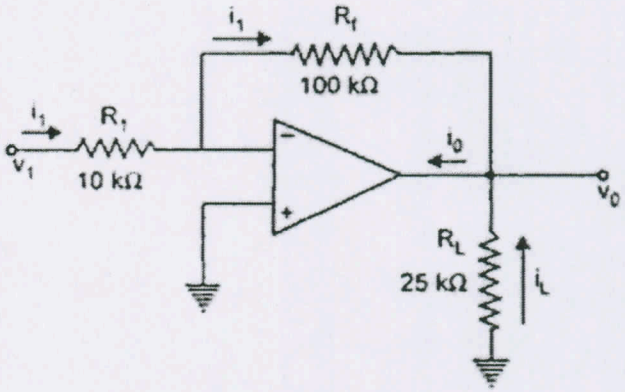

Figure-7

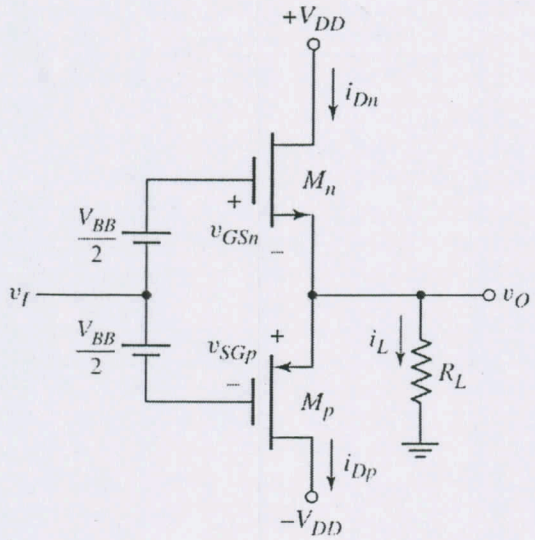

Figure-8

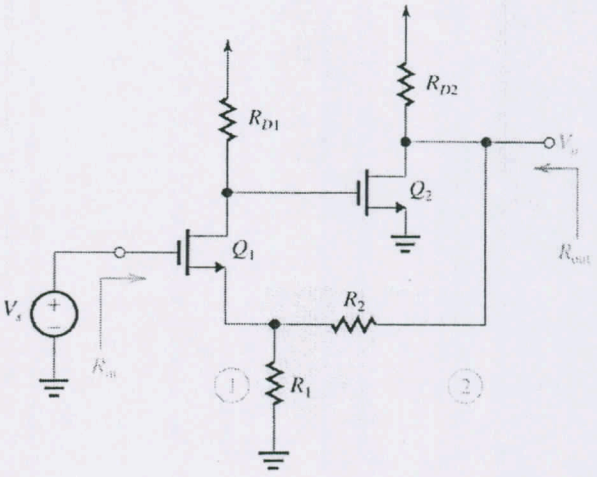

Figure-9